UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,625	10/24/2001	Federico Pio	854063.512D1	1452

500 7590 10/07/2003

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVE
SUITE 6300
SEATTLE, WA 98104-7092

EXAMINER	
KANG, DONGHEE	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/001,625	PIO, FEDERICO	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-15 and 17-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,5-8,15 and 17-20* is/are allowed.

6)☒ Claim(s) *9-14, 21, 23-26, 28-30 and 32-33* is/are rejected.

7)☒ Claim(s) *22,27 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other

DETAILED ACTION

Remarks

1. Applicant's Amendment and Response to Paper No.3 have been entered and made of Record. Claims 4 & 16 are cancelled and new claims 21-33 are added. Thus, claims 1-3, 5-15 & 17-33 are pending in this application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims **9, 10 & 12** are rejected under 35 U.S.C. 102(b) as being anticipated by Jiang et al. (US 5,773,314).

Re claims **9, 21 & 25**, Jiang et al. teach a method of forming an integrated semiconductor structure having a plurality of connection levels, comprising (Fig.8):

forming a first conductive region (34); forming a first insulating layer (42) having an upper surface over the first conductive region; etching a first opening through the first insulating layer (Fig.2) to expose a portion of the first conductive region; forming a first conductive plug (44) that fills the first opening and is electrically coupled to the first conductive region, the first conductive plug having an upper surface extending no

further than the upper surface of the first insulating layer; forming a second insulating layer (58) having an upper surface over the first insulating layer; etching a second opening through the second insulating layer to expose a portion of the upper surface of the first conductive plug; forming a second conductive plug (60) that fills the second opening and is electrically coupled to the first conductive plug, the second conductive plug directly contacting the upper surface of the first conductive plug, and further having an upper surface extending no further than the upper surface of the second insulating layer; forming a third opening through the first insulating layer; forming a third conductive plug (46, Fig.2) that fills the third opening and has an upper surface extending no further than the upper surface of the first insulating layer, the first and third conductive plugs being formed simultaneously; forming a fourth opening through the second insulating layer in a position not directly above the third conductive plug; forming a fourth conductive plug (60) that fills the fourth opening, second and fourth conductive plugs being formed simultaneously; forming a second conductive region over the first insulating layer, the second conductive region directly electrically coupling the third conductive plug to the fourth conductive plug; and forming, above the second insulating, a third conductive region (122) aligned and in direct contact with the second through region.

Re claim **10**, Jiang et al. teach forming the first conductive region comprises implanting a dopant into a substrate over which the first insulating layer is formed (Col.4, lines 15-16).

Re claim **12**, Jiang et al. teach forming the first conductive plug comprises:

depositing a conductive layer over the first insulating layer and filling the first opening; and

removing the conductive layer over the first insulating layer by polishing to leaving conductive material filling the first conductive via.

4. Claims **9, 11, 21, 24, 26, & 29** are rejected under 35 U.S.C. 102(e) as being anticipated by Kim (US 6,448,651).

Kim teaches a method of forming an integrated semiconductor structure having a plurality of connection levels, comprising (Fig.3):

forming a first conductive region (104); forming a first insulating layer (106) having an upper surface over the first conductive region; etching a first opening through the first insulating layer (Fig.3a) to expose a portion of the first conductive region; forming a first conductive plug (108b) that fills the first opening and is electrically coupled to the first conductive region, the first conductive plug having an upper surface extending no further than the upper surface of the first insulating layer; forming a second insulating layer (116) having an upper surface over the first insulating layer; etching a second opening through the second insulating layer to expose a portion of the upper surface of the first conductive plug (Fig.3b); forming a second conductive plug (60) that fills the second opening and is electrically coupled to the first conductive plug (118b), the second conductive plug directly contacting the upper surface of the first conductive plug, and further having an upper surface extending no further than the upper surface of the second insulating layer; forming a third opening through the first

insulating layer; forming a third conductive plug (108a) that fills the third opening and has an upper surface extending no further than the upper surface of the first insulating layer, the first and third conductive plugs being formed simultaneously; forming a fourth opening through the second insulating layer in a position not directly above the third conductive plug; forming a fourth conductive plug (118a) that fills the fourth opening, second and fourth conductive plugs being formed simultaneously; forming a second conductive region (110) over the first insulating layer, the second conductive region directly electrically coupling the third conductive plug to the fourth conductive plug; forming an etch stop layer (114) on the second conductive region and the first insulating region; and forming, above the second insulating, a third conductive region (122) aligned and in direct contact with the second through region, wherein forming the first conductive region comprising depositing a semiconductor material prior to forming the first insulating layer.

5. Claims **21, 23-24, 26, 28, 30 & 32-33** are rejected under 35 U.S.C. 102(e) as being anticipated by Matsuoka et al. (US 6,130,449).

Re claim **21**, Matsuok et al. teach a method for manufacturing an integrated semiconductor device, having a plurality of connection levels, comprising (Fig.1):

forming a first conductive region inside a substrate of semiconductor material (1); forming a first insulating region (9) of dielectric material above the first conductive region; forming a first through region of electrically conductive material inside the first insulating region, and in direct electrical contact with the first conductive region; forming

a conductive layer on the first insulating region (601, Fig.13); etching the conductive layer to remove all of the conductive layer directly above the thirst through regionand simultaneously form a second conductive region (Fig.14) in a position not aligned and not in contact with the first through region; forming a second insulating region (901, Fig.15) of dielectric material, covering the second conductive region; forming, inside the second insulating region, a second through region of electrical conductive material (Fig.17), extending as far as the first through region, aligned and in direct electrical contact with the first through region; and forming, above the second insulating region, a third conductive region (Fig.25) aligned and in direct electrical contact with the second through region.

Re claim **23**, Matsuok et al. teach the method further comprising forming an etch stop layer (Fig.15) of a first dielectric material on the second conductive region and the first insulating region, wherein the second insulating region is formed of a second dielectric material different than the etch stop layer, and the second through region is formed through the etch stop layer and the second insulating region.

Re claim **24**, Matsuok et al. teach the method further comprising:

forming a third through region of electrically conductive material inside the first insulating region and spaced apart from the first through region, the first and third through regions being formed simultaneously; forming, inside the second insulating region, a fourth through region of electrically conductive material, extending as far as the third through region, aligned and in direct electrical contact with the third through region, the third and fourth through regions being formed simultaneously, wherein the

second conductive region is spaced apart from and positioned between the third and fourth through regions.

Re claim **26**, Matsuoka et al. teach a method for manufacturing an integrated semiconductor device, having a plurality of connection levels, comprising (Fig.1):

forming a first conductive region inside a substrate of semiconductor material; forming a first insulating region of dielectric material (9) above the first conductive region; forming a first through region of electrically conductive material inside the first insulating region, and in direct electrical contact with the first conductive region; forming a second conductive region (Fig.16) above the first insulating region, in a position not aligned and not in contact with the first through region; forming an etch stop layer (Fig.15) of a first dielectric material on the second conductive region and the first insulating region; forming on the etch stop layer a second insulating region (901) of a second dielectric material different than the etch stop layer; forming, inside the etch stop layer and the second insulating region, a second through region of electrically conductive material (Fig.17), extending as far as the first through region, aligned and in direct electrical contact with the first through region; and forming, above the second insulating region, a third conductive region (Fig.22) aligned and in direct electrical contact with the second through region.

Re claim **28**, Matsuoka et al. teach the method further comprising:

forming a third through region of electrically conductive material inside the first insulating region and spaced apart from the first through region, the first and third through regions being formed simultaneously; forming, inside the second insulating

region, a fourth through region of electrically conductive material, extending as far as the third through region, aligned and in direct electrical contact with the third through region, the second and fourth through regions being formed simultaneously, wherein the second conductive region is spaced apart from and positioned between the second and fourth through regions.

Re claim **30**, Matsuoka et al. teach a method for manufacturing an integrated semiconductor device, having a plurality of connection levels, comprising (Fig.1):

Forming a first conductive region inside a substrate of semiconductor material; forming a first insulating region of dielectric material (9) above the first conductive region; forming a first through region of electrically conductive material inside the first insulating region, and in direct electrical contact with the first conductive region; forming a second through region of electrically conductive material inside the first insulating region, the first and second through regions being formed simultaneously; forming a second conductive region above the first insulating region, in a position between and not on contact with the first and second through regions; forming a second insulating region of dielectric material, covering the second conductive region; forming through the second insulating region, a third through region of electrically conductive material, extending as far as the first through region, aligned and in direct electrical contact with the first through region; and forming, through the second insulating region, a fourth conductive region aligned and in direct electrical contact with the second through region, the third and fourth conductive regions being formed simultaneously after forming the second insulating region above the second conductive region.

Re claim **32**, Matsuoka et al. teach the method further comprising forming an etch stop layer of a first dielectric I material on the second conductive region and the first insulating region, wherein the second insulating region is formed of a second dielectric material different than the etch stop layer, and the third and fourth through regions are formed through the etch stop layer and the second insulating region.

Re claim **33**, Matsuoka et al. teach the second insulating region is a single layer that covers the second conductive region and separates the second conductive region from the third and fourth through regions.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims **13-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. in view of Tsui (US 5,891,799).

Jiang et al. teach substantially the entire claimed invention, as applied to claim 9 explained above, except that forming the second insulating layer comprises:

forming a first dielectric layer over the first conductive region; and forming a second dielectric layer over the first dielectric layer,

wherein the second insulating layer comprises etching through the second dielectric layer and subsequently etching the first dielectric layer.

However, Tsui teaches in Fig.11 & Col.7, lines 1-22 that forming the second insulating layer comprises forming a first dielectric layer (SiO_2, 14') over the first conductive region (12); and forming a second dielectric layer (Si_3N_4, 16') over the first dielectric layer (14'), wherein the second insulating layer comprises etching through the second dielectric layer (16') and subsequently etching the first dielectric layer (14') to form a via hole in which a patterned second conductive plug (4') is later formed for the next level of metal line.

Therefore it would have been obvious to one of ordinary skill in the art of making semiconductor device to apply the teaching of Tsui in the method of Bandyopadhyay et al., to form a silicon nitride layer on the silicon oxide layer in order to provide an etch stop layer when the second conductive plug is formed by a chemical mechanical polishing (CMP) process so that the surface of the second conductive plug can be substantially flush with the surface of the silicon nitride film. This invention allows for the stacking of vias to further reduce the integrated circuit area.

Allowable Subject Matter

8. Claims 1-3, 5-8, 15 & 17-20 are allowed.

9. Claims 22, 27 & 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance and indicating allowable subject matter:

Prior art reference, taken along or in combination, do not teach or render obvious that the first conductive region is of metal material, a third insulating region extends above the substrate, and the first conductive region extends above the third insulating region.

Response to Arguments

10. Applicant's arguments with respect to claims 9-14, 21, 23-26, 28-30 & 32-33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

dhk

Tom Thomas

TOM THOMAS

SUPERVISORY PATENT EXAMINER